IN THE CLAIMS

Amend the claims as follows:

- 1. (Original) A dynamic semiconductor memory device, comprising:
- a memory cell array including a plurality of memory cells, the memory cell array being divided into a plurality of blocks;
 - a block decoder for decoding row address signals and producing block selection signals;
- a refresh cycle control circuit for dividing the block selection signals by preset frequency dividing ratios to set refresh cycles for the blocks; and
 - a row decoder for selecting the blocks in response to the block selection signals.
- 2. (Original) The dynamic semiconductor memory device according to Claim 1, wherein the refresh cycle control circuit comprises:
 - a fuse circuit for setting the frequency dividing ratios; and
- a frequency divider for dividing the block selection signals by frequency dividing ratios set in the fuse circuit.
- 3. (Original) The dynamic semiconductor memory device according to Claim 2, wherein the fuse circuit is formed on the row decoder.
- 4. (Currently Amended) A dynamic semiconductor memory device comprising:
- a memory cell array including a plurality of memory cells, the memory cell array being divided into a plurality of first hierarchical blocks and each of the first hierarchical blocks being further divided into a plurality of second hierarchical blocks; and
- a refresh cycle setting means for setting circuit configured to set a first refresh cycle for the first hierarchical blocks and a second refresh cycle for the second hierarchical blocks.
- 5. (Currently Amended)The dynamic semiconductor memory device according to Claim 4, further comprising:
- a row decoder for selecting one of the first hierarchical blocks in response to a first block selection signal and for selecting one of the second hierarchical blocks in the selected first hierarchical block in response to a second block selection signal,
 - wherein the refresh cycle setting means circuit comprises:
 - a first frequency divider for dividing the first block selection signal by a predetermined first

frequency dividing ratio; and

a second frequency divider for dividing the second block selection signal by a predetermined second frequency dividing ratio.

- 6. (Currently Amended) The dynamic semiconductor memory device according to Claim 5, wherein the refresh cycle setting means circuit further comprises: a first fuse circuit for setting the first frequency dividing ratio; and
- a second fuse circuit for setting the second frequency dividing ratio.
- 7. (Original) The dynamic semiconductor memory device according to Claim 6, wherein the first and second fuse circuits are formed on the row decoder.
- 8. (Currently Amended) The dynamic semiconductor memory device according to Claim 4, further comprising:

a row decoder for selecting one of the first hierarchical blocks in response to a first block selection signal and for selecting one of the second hierarchical blocks in the selected first hierarchical block in response to a second block selection signal,

wherein the refresh cycle setting means circuit comprises:

- a frequency divider for dividing the second block selection signal by a predetermined first or second frequency dividing ratio.
- 9. (Currently Amended) The dynamic semiconductor memory device according to Claim 8, wherein the refresh cycle setting means circuit further comprises:
 - a fuse circuit for setting the first or second frequency dividing ratio.
- 10. (Original) The dynamic semiconductor memory device according to Claim 9, wherein the fuse circuit is formed on the row decoder.
- 11. (New) A method of selectively controlling a refresh cycle time of a dynamic semiconductor memory device, comprising:

dividing a memory cell array including a plurality of memory cells into a plurality of blocks;

decoding row address signals and a plurality of producing block selection signals;

dividing the block selection signals by preset frequency dividing ratios to set refresh cycles for the blocks using a refresh cycle control circuit; and

selecting the blocks in response to the block selection signals with a row decoder.

12. (New) The method according to Claim 11, further comprising:

setting the frequency dividing ratios with a fuse circuit; and

dividing the block selection signals by frequency dividing ratios set in the fuse circuit using a frequency divider.

13. (New) The method according to Claim 12, further comprising forming the fuse circuit on the row decoder.